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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/710,057	11/10/2000	Becky Cavanaugh	62061.0105	4116

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609 Castle Ridge Road  
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EXAMINER

DAMIANO, ANNE L

ART UNIT	PAPER NUMBER
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2184

DATE MAILED: 10/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Applicati n N .

09/710,057

Applicant(s)

CAVANAUGH ET AL.

Examin r

Anne L Damiano

Art Unit

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-- The MAILING DATE of this c mmunication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 10 November 2000.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-30 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-30 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 10 November 2000 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)                      4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)                      5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 4 .                      6) ☐ Other:

## **DETAILED ACTION**

### ***Drawings***

1. Figures 1 and 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

### ***Specification***

2. The disclosure is objected to because of the following informalities:

The applications and patents made reference to (page 15, lines 18 and 19, page 16, line 22, and page 17, line 2) are lacking their respective numbers.

Appropriate correction is required.

### ***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claims 1-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Chin et al. (6,484,135).

As in claims 1, 6, 11, 16 and 21, Chin discloses a processor verification test apparatus and system, implementing a method which is stored on a program storage device readable by a computer that tangibly embodies a program of instructions executable by the computer to perform the method (column 9: lines 32-37), that uses a golden model (hardware emulator) to generate a test that verifies that a processor system under test (hardware model) properly executes two or more instructions issued and executed in parallel, comprising:

A user preference queue (user-defined directives) that comprises queue entries wherein each queue entry further comprises an instruction to be tested, a group or tree of instructions to be tested, or a test generator control command (figure 4, column 4: lines 10-14 and column 6: lines 35-65) (The user-defined directives include instruction type directives (column 6: line 59, figure 4: component 116));

A plurality of resource-related data structures, wherein each of the resource-related data structure comprises information concerning selected system resources of the golden model (hardware emulator), wherein the information comprises one or more of the following: actual past state, actual present state, actual future state, predicted past state, predicted present state, or predicted future state (column 3: lines 9-11, column 5: lines 4-6 and 9-12) (The internal state information is the same as an actual present state resource related data structure.);

An instruction packer (test generator) coupled to the user preference queue (verification directives, figure 3: component 81) and the resource-related data structures (feedback of internal state information, figure 3: component 97), the instruction packer creating a group of N instructions (test vectors) valid for parallel execution by the golden model (hardware emulator) and the processor system under test (hardware model) (column 5: lines 14-16), where N equals 1 or more (figure 3: component 82, 84, 97, column 6: lines 52-56 and column 10: lines 1-12) (The test generator tailoring the generation of future test vectors based on feedback of actual present state resource related data structure is interpreted as creating a group of instructions valid for parallel execution by the golden model and the processor system under test.); and

An instruction generator and simulator (model simulator) that generates and simulates instructions that correspond to the group of N instructions created by the instruction packer, evaluates the updated architectural state of the golden model, and updates the resource-related data structures (internal state information within the hardware emulator is updated) (column 9: lines 2-9).

As in claims 2, 7, 12, 17, and 22, Chin discloses the processor verification test apparatus and system, implementing a method which is stored on a program storage device readable by a computer that tangibly embodies a program of instructions executable by the computer to perform the method, wherein the group of N instructions valid for parallel execution further comprises N instructions that do not utilize common system resources other than source registers of the golden model or processor system under test (column 6: lines 52-56, column 7: lines 57-59 and line 66-column 8: line 5). (The test generator tailoring the generation of future test vectors based on feedback of actual present state resource related data structure is interpreted as ensuring that the instructions do not utilize common system resources. Also, more specifically, the address conflict directive, directing the test generator to avoid address conflicts, is interpreted as the instructions not utilizing common system resources other than source registers.)

As in claims 3, 8, 13, 18, and 23, Chin discloses the processor verification test apparatus and system, implementing a method which is stored on a program storage device readable by a computer that tangibly embodies a program of instructions executable by the computer to perform the method, wherein the instruction packer creates that group of N instructions valid for parallel execution by selecting instructions from an instruction tree in the user preference queue, wherein the instruction packer iteratively creates a group of potentially valid instructions by eliminating instructions

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ineligible for selection, based upon information indicated by the resource-related data structures and the instruction grouping rules for the golden model and the processor system under test (figure 3: component 82, 84, 97, column 6: lines 52-56 and column 10: lines 1-12) (The test generator tailoring the generation of future test vectors based on feedback of actual present state resource related data structure is interpreted as eliminating instructions ineligible for selection, based upon information indicated by the resource-related data structures.)

As in claims 4, 9, 14, 19 and 24, Chin discloses the processor verification test apparatus and system, implementing a method which is stored on a program storage device readable by a computer that tangibly embodies a program of instructions executable by the computer to perform the method, wherein the group of N instructions further comprises at least a first instruction and a second instruction wherein the second instruction is selected from the group of potentially valid instructions, and wherein the second instruction further comprises an instruction that does not utilize the same system resources other than source registers utilized by the first instruction (column 6: lines 52-56, column 7: lines 57-59 and line 66-column 8: line 5, and column 8: line 65-column 9: line 21) (The test generator tailoring the generation of future test vectors based on feedback of actual present state resource related data structure is interpreted as the second instruction not utilizing the same system resource that is used by the first instruction. Also, more specifically, the system avoids address conflicts, and proceeding

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if a conflict does not exist (column 8: line 1-9), is the first instruction not utilizing the same system resource that is used by the first instruction.)

As in claims 5, 10, 15, 20, and 25, Chin discloses the processor verification test apparatus and system, implementing a method which is stored on a program storage device readable by a computer that tangibly embodies a program of instructions executable by the computer to perform the method, wherein the instruction packer creates that group of N instructions valid for parallel execution by selecting instructions in one of the following ways:

By selecting each instruction in the order that the instruction appears in an ordered instruction list in the user preference queue, or by selecting a "no operation" instruction (no read operation) where the next instruction in the ordered instruction list requires unavailable system resources or violates the processor grouping rules (column 8: lines 50-57).

Claim 26 is substantially similar in scope to the combination of claims 1-5 and therefore are rejected under similar rational.

Claim 27 is substantially similar in scope to the combination of claims 6-10 and therefore are rejected under similar rational.

Claim 28 is substantially similar in scope to the combination of claims 11-15 and therefore are rejected under similar rational.

Claim 29 is substantially similar in scope to the combination of claims 16-20 and therefore are rejected under similar rational.

Claim 30 is substantially similar in scope to the combination of claims 21-25 and therefore are rejected under similar rational.

### ***Conclusion***

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

See PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anne L Damiano whose telephone number is (703) 305-8010. The examiner can normally be reached on M-F 9:00AM-6:30PM, first Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (703) 305-9731. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

ALD  
September 22, 2003



**SCOTT BADERMAN**  
**PRIMARY EXAMINER**